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Methods Of Forming Polished Material And Methods Of Forming Isolation Regions

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Methods Of Forming Polished Material And Methods Of Forming Isolation Regions

TECHNICAL FIELD

The invention pertains to methods of forming polished material, such as, for example, methods of forming isolation regions.

BACKGROUND OF THE INVENTION

In modern semiconductor device applications, millions of individual devices are packed onto a single small area of a semiconductor substrate, and many of these individual devices may need to be electrically isolated from one another. One method of accomplishing such isolation is to form a trenched isolation region between adjacent devices. Such trenched isolation region will generally comprise a trench or cavity formed within the substrate and filled with an insulative material, such as silicon dioxide.

A prior art method for forming trench isolation regions is described with reference to Figs. 1-10. Referring to Fig. 1, a semiconductive wafer fragment 10 is shown at a preliminary stage of a prior art processing sequence. Wafer fragment 10 comprises a semiconductive material 12 having an upper surface 13. A layer of silicon dioxide 14 is formed over upper surface 13, and a layer of silicon nitride 16 is formed over silicon dioxide 14. A patterned masking layer 18 is formed over silicon nitride 16.

Substrate 12 can comprise, for example, monocrystalline silicon lightly doped with a conductivity enhancing material. For purposes of interpreting this document and the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Silicon dioxide layer 14 has a typical thickness of about 90Å, nitride layer 16 has a typical thickness of from about 700Å to about 800Å, and masking layer 18 has a typical thickness of about 10,000Å. Nitride layer 16 comprises a lower surface 15 and an upper surface 17. Patterned masking layer 18 can comprise, for example, photoresist.

Referring to Fig. 2, a pattern is transferred from layer 18 to nitride layer 16 and oxide layer 14 to form masking blocks 20 over substrate 12. Blocks 20 are separated by intervening openings (also referred to as trenches or gaps) 22, 24, 26, 28 and 30. Gaps 22, 24, 26, 28 and 30 define locations wherein isolation regions will ultimately be formed. In the shown typical embodiment, gaps 22, 24, 26, 28 and 30 vary in width, with gap 26 representing a wide trench. The

variation in width of gaps 22, 24, 26, 28 and 30 is a matter of discretion for persons fabricating devices over substrate 12. Such variation in width is shown to exemplify how particular problems associated with polishing processes (the problems are discussed below) become exaggerated at wider trench openings.

Referring to Fig. 3, openings 22, 24, 26, 28 and 30 are extended into substrate 12. The processing of Figs. 2 and 3 typically occurs in a single etch step.

Referring to Fig. 4, photoresist material 18 (Fig. 3) is removed. Subsequently, an insulative material 40 is provided to fill the trenches 22, 24, 26, 28 and 30. Insulative material 40 typically comprises silicon dioxide, and can be formed by, for example, high density plasma deposition. The term "high density" as used in this document to refer to a deposition plasma means a deposition plasma having a density of greater than 10^{10} ions/cm^3. The outer surface of the deposited insulative material 40 comprises surface peaks 42 (which actually have a three-dimensional pyramid shape) extending over the patterned nitride material 16. Peaks 42 result as an aspect of high density plasma deposition.

Referring to Fig. 5, wafer fragment 10 is subjected to a polishing process to remove insulative material 40 from over nitride layer 16, and to thereby remove peaks 42 (Fig. 4) and polish the insulative material 40 down to about even with an upper surface of nitride 16. After the

polishing process, insulative material 40 forms isolation regions 50, 52, 54, 56 and 58 within openings 22, 24, 26, 28 and 30, respectively. The isolation regions and silicon nitride layer 16 comprise a coextensive upper surface 60. Upper surface 60 can be at about a same elevational level as original upper surface 17 (Fig. 1) of nitride layer 16, or can be below such elevational level, depending on whether the polishing process has removed any of the material of silicon nitride layer 16. Generally, the polishing process removes some of silicon nitride layer 16, but will slow significantly upon reaching silicon nitride layer 16 such that silicon nitride layer 16 effectively functions as an etch stop layer to define an end point of the polishing process. Exemplary polishing processes include chemical-mechanical polishing, as well as dry and wet etches selective for silicon dioxide relative to silicon nitride. In particular applications, insulative material 40 comprises silicon dioxide and is polished down to a level that is above the upper surface of the silicon nitride. The material 40 is then brought to about level with the upper surface of the silicon nitride with a subsequent wet acid (hydrofluoric acid) dip.

Ideally, upper surface 60 will be substantially planar. However, as shown a problem frequently occurs during the polishing of insulative material 40 wherein concavities 62 occur at the top of isolation regions 50, 52, 54, 56 and 58. Such problem is commonly referred to as "dishing." The problem is frequently more severe at wider isolation

regions, corresponding to wider trenches, (i.e., isolation region 54) than at narrower isolation regions (i.e., isolation regions 50, 52, 56 and 58). The dishing can become particularly pronounced for isolation regions having widths greater than or equal to about 5 microns.

Referring to Figs. 6 and 7, nitride layer 16 (Fig. 5) is removed, and subsequently pad oxide 14 is stripped. The stripping of pad oxide layer 14 can be accomplished with a hydrofluoric acid dip. Such dip also removes some of the silicon oxide from isolation regions 50, 52, 54, 56, and 58, and accordingly reduces a height of the oxide in such isolation regions.

Referring to Fig. 8, a sacrificial silicon dioxide layer 19 is formed over substrate 12. Such sacrificial silicon dioxide layer can be grown from silicon of substrate 12, or deposited over substrate 12.

Referring to Fig. 9, sacrificial silicon dioxide layer 19 is stripped from over substrate 12. The stripping of sacrificial silicon dioxide layer 19 can be accomplished with a hydrofluoric acid dip. Such dip also removes some of the silicon oxide from isolation regions 50, 52, 54, 56, and 58, and accordingly reduces a height of the oxide in such isolation regions.

Referring to Fig. 10, a gate oxide layer 21 is formed over substrate 12. Such gate oxide layer can be grown from silicon of substrate 12, or deposited over substrate 12. It is noted that only pertinent processing steps are discussed in describing Figs. 8-10, and that

additional processing steps (in addition to those discussed) can occur between the forming of the sacrificial oxide layer and the forming of the gate oxide layer.

As shown in Fig. 10, the dishing described with reference to Fig. 5 can remain in isolation regions 50, 52, 54, 56 and 58 after the processing of Figs. 6-10, and can result in at least some of the isolation regions having portions below an elevational level of the upper surface of substrate 12. The dishing also causes the isolation regions to have corners 70 which are not right angles. Such corners 70 can undesirably affect operating voltages of devices formed proximate isolation regions 50, 52, 54, 56 and 58, and can, for example, result in non-uniformity of threshold voltages for such devices. It would therefore be desirable to develop alternative methods of forming isolation regions.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a polished material. A substrate is provided and an elevational step is provided relative to the substrate. The elevational step has an uppermost surface. A material is formed beside the elevational step. The material extends to above the elevational step uppermost surface and has lower and upper layers. The lower layer polishes at slower rate than the upper layer under common polishing conditions. The lower layer joins the upper layer at an interface. The material is polished down to about the elevational level of the elevational step uppermost surface utilizing the common polishing conditions.

In another aspect, the invention encompasses a method of forming an isolation region. A substrate is provided. The substrate has an opening extending therein and a surface proximate the opening. A material is formed within the opening. The material extends to above the substrate surface, and comprises a lower layer and an upper layer. The lower layer is more dense than the upper layer, and joins the upper layer at an interface that extends to at or below an elevational level of the substrate surface. The material is polished at least down to about the elevational level of the substrate surface.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a schematic, cross-sectional, fragmentary view of a semiconductor wafer fragment at a preliminary processing step in accordance with a prior art processing sequence.

Fig. 2 shows the Fig. 1 wafer fragment at a prior art processing step subsequent to that of Fig. 1.

Fig. 3 shows the Fig. 1 wafer fragment at a prior art processing step subsequent to that of Fig. 2.

Fig. 4 shows the Fig. 1 wafer fragment at a prior art processing step subsequent to that of Fig. 3.

Fig. 5 shows the Fig. 1 wafer fragment at a prior art processing step subsequent to that of Fig. 4.

Fig. 6 shows the Fig. 1 wafer fragment at a prior art prior art processing step subsequent to that of Fig. 5.

Fig. 7 shows the Fig. 1 wafer fragment at a prior art prior art processing step subsequent to that of Fig. 6.

Fig. 8 shows the Fig. 1 wafer fragment at a prior art prior art processing step subsequent to that of Fig. 7.

Fig. 9 shows the Fig. 1 wafer fragment at a prior art prior art processing step subsequent to that of Fig. 8.

Fig. 10 shows the Fig. 1 wafer fragment at a prior art prior art processing step subsequent to that of Fig. 9.

Fig. 11 is a schematic, fragmentary, cross-sectional view of a semiconductive wafer fragment in process according to a method of the present invention. The wafer fragment of Fig. 11 is shown at a processing step subsequent to that of prior art Fig. 3.

Fig. 12 shows the Fig. 11 wafer fragment at a processing step subsequent to that of Fig. 11.

Fig. 13 shows the Fig. 11 wafer fragment at a processing step subsequent to that of Fig. 12.

Fig. 14 shows the Fig. 11 wafer fragment at a processing step subsequent to that of Fig. 13.

Fig. 15 shows the Fig. 11 wafer fragment at a processing step subsequent to that of Fig. 14.

Fig. 16 shows the Fig. 11 wafer fragment at a processing step subsequent to that of Fig. 15.

Fig. 17 shows the Fig. 11 wafer fragment at a processing step subsequent to that of Fig. 16.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

An exemplary embodiment of the invention is described with reference to a semiconductive wafer fragment 10a in Figs. 11-17 as a method of forming field isolation regions. However, it is to be understood that the invention has applications beyond formation of field isolation regions and can, for example, be applied generally to polishing processes. In referring to Figs. 11-17, similar numbering to that utilized above in describing the prior art will be used, with differences indicated by the suffix "a", or by different numerals.

Referring to Fig. 11, semiconductive wafer fragment 10a is shown at a processing step subsequent to that of the step described above with reference to prior art Fig. 3. Semiconductive wafer fragment 10a comprises a substrate 12 over which a silicon dioxide layer 14 and a silicon nitride layer 16 are provided. Silicon nitride layer 16 can be referred to herein as an etchstop layer. Openings 22, 24, 26, 28 and 30 extend through layers 14 and 16 and into substrate 12. An insulative material 100 is formed over substrate 12 and within openings 22, 24, 26, 28 and 30. It is noted that wafer fragment 10a of Fig. 11 is shown at a processing step similar to that of wafer fragment 10 of Fig. 4. However, wafer fragment 10a of Fig. 11 differs from the wafer

fragment 10 of Fig. 4 in that insulative material 100 comprises two distinct layers (or regions) 102 and 104, whereas insulative material 40 (Fig. 4) comprises only a single layer.

Layers 102 and 104 of insulative material 100 join at an interface 106 which is indicated by a dashed line, and differ from one another in that layer 102 comprises a different density than layer 104. Preferably, the lower layer (layer 102) is denser than the upper layer (layer 104). Interface 106 preferably extends from above silicon nitride layer 16 to at or below an elevational level of upper surface 17 of silicon nitride layer 16. Interface 106 comprises uppermost portions 112 and lowermost portions 114. Preferably, lowestmost portions 114 are elevationally at a level that is at least about as high as an elevational level of upper surface 13 of substrate 12, and no higher than an elevational level of upper surface 17 of silicon nitride layer 16. However, it is to be understood that in particular embodiments such lowermost portions 114 can be above the elevational level of upper surface 17 of nitride layer 16.

Layers 102 and 104 can comprise a common material, with the only difference between layers 102 and 104 being the difference in density. For instance, layers 102 and 104 can both comprise high density plasma deposited silicon dioxide. The difference in density can be expressed as a different in wet etch rate. For instance, in a preferred embodiment, the denser lower layer 102 will etch in a wet

oxide etch at a rate that is from about 1 times the etch rate of thermal oxide to about 1.3 times the etch rate of thermal oxide. In contrast, the less dense upper layer 104 will etch in a wet oxide etch at a rate that is from about 1.5 times the etch rate of thermal oxide to about 2.5 times the etch rate of thermal oxide. The described wet etch can comprise dilute HF (i.e., 300:1 water:hydrofluoric acid), at room temperature. It is to be understood that the above-described wet etch rates are merely methods of quantitating the relative densities of layers 102 and 104, and do not imply that the layers are subjected to a wet etch in methods of the present invention.

An exemplary method of forming high density plasma deposited silicon dioxide having a first layer 102 formed to be a higher density silicon dioxide than a second layer 104 is as follows. Initially, first layer 102 is formed utilizing a high density plasma, a pressure of from 0.1 mTorr to about 1 Torr, and a power of from about 1,000 watts to about 3,000 watts, with the power representing both radio frequency and bias. The reaction occurs in a deposition chamber into which silane is flowed at a rate of from about 50 standard cubic centimeters per minute (sccm) to about 150 sccm, with a preferred flow rate of about 100 sccm. Oxygen (O_2) is flowed into the chamber at a rate of from about 50 sccm to about 150 sccm, with a preferred rate of about 100 sccm, and argon is flowed into the chamber at a rate of from about 400 sccm to about 600 sccm, with a preferred rate of about 500 sccm.

Substrate 12 is maintained at a temperature of from about 500°C to about 700°C, and preferably about 600°C, by flowing helium against a backside of substrate 12. After formation of layer 102 to a desired depth, the temperature of the wafer is dropped to less than or equal to 400°C (preferably to from about 300°C to about 400°C) and second layer 104 is deposited. The temperature can be dropped by increasing a flow of helium against a backside of substrate 12.

Insulative material 100 comprises peaks 120 over silicon nitride layer 16, and valleys over openings 22, 24, 26, 28 and 30. In accordance with one aspect of the invention, it is recognized that material 100 polishes faster from peaks 120 than from lower regions due to a lesser volume of material to polish. Also, it is recognized that the portion of material 100 comprised by denser layer 102 will generally polish at a slower rate than the less dense portion of material 100 comprised by layer 104. Accordingly, as material 100 is subjected to a polishing process the initially faster polishing rate of peaks 120, combined with the relatively faster polishing rate of layer 104 relative to layer 102, can result in planarity occurring at an upper surface of material 100 during the polishing process. The elevational location of the upper surface of material 100 at which such planarity is achieved can be adjusted by one or more of (1) altering the elevational location of interface 106; and (2) altering the relative density of portions 102 and 104. Preferably, planarity of the upper surface of material 100 occurs

when the upper surface of material 100 coincides to at or about lower portion 114 of interface 106. Alternatively, such planarity can occur when the upper surface of material 100 is about even with upper surface 17 of nitride layer 16.

Fig. 12 illustrates wafer fragment 10a after being subjected to a polishing process. Wafer fragment 10a comprises a plurality of isolation regions 50a, 52a, 54a, 56a and 58a, each of which contains insulative material 100. Wafer fragment 10a further comprises a substantially planar upper surface 60a which is coextensive across an upper surface of silicon nitride layer 16 and upper surfaces of isolation regions 50, 52a, 54a, 56a and 58a. In the shown preferred embodiment, upper surface 60a is at or about an elevational level of lower portions 114 (Fig. 11) of interface 106 (Fig. 11). Accordingly, isolation regions 50a, 52a, 54a, 56a and 58a comprise primarily the higher density silicon dioxide of layer 102 (Fig. 11), rather than the lower density silicon dioxide of layer 104 (Fig. 11). Such incorporation of primarily higher density silicon dioxide can eliminate a high density plasma densification anneal utilized for treating isolation regions formed in accordance with the prior art.

Although the above described planarization was accomplished utilizing layers 102 and 104 (Fig. 11) which differed in density, it will be appreciated that such can be generally accomplished utilizing layers 102 and 104 which differ in polishing rate under common polishing

conditions. By "common polishing conditions" it is meant conditions which are identical with respect to both of layers 102 and 104. Accordingly, the term "common polishing conditions" encompasses procedures in which both of layers 102 and 104 are exposed to the same polish at the same time, as well as procedures wherein the compositions of layers 102 and 104 are exposed to identical polishing conditions at different times. The description of layers which "differ in polishing rate under common polishing conditions" is used herein to describe relative physical properties of layers 102 and 104, and does not indicate particular polishing procedures applied to layers 102 and 104.

Referring to Figs. 13 and 14, nitride layer 16 (Fig. 12) is removed, and subsequently pad oxide 14 is stripped. The stripping of pad oxide layer 14 can be accomplished with a hydrofluoric acid dip. Such dip also removes some of the silicon oxide from isolation regions 50a, 52a, 54a, 56a, and 58a, and accordingly reduces a height of the oxide in such isolation regions.

Referring to Fig. 15, a sacrificial silicon dioxide layer 19 is formed over substrate 12. Such sacrificial silicon dioxide layer can be grown from silicon of substrate 12, or deposited over substrate 12.

Referring to Fig. 16, sacrificial silicon dioxide layer 19 (Fig. 15) is stripped from over substrate 12. The stripping of sacrificial silicon dioxide layer 19 can be accomplished with a hydrofluoric acid dip. Such dip also removes some of the silicon oxide from isolation regions 50a,

52a, 54a, 56a, and 58a, and accordingly reduces a height of the oxide in such isolation regions.

Referring to Fig. 17, a gate oxide layer 21 is formed over substrate 12. Such gate oxide layer can be grown from silicon of substrate 12, or deposited over substrate 12. Isolation regions 50a, 52a, 54a, 56a and 58a of Fig. 17 have corners 70a which, unlike the corners 70 of the prior art construction (Fig. 10), are substantially right angles.

The terminology utilized above in describing Figs. 11-17 is but one of many ways in which a method of the present invention can be described. For instance, the above description referred to the bulk mass labeled 12 as a substrate, and to the masses labeled 14 and 16 as layers over the substrate 12. An alternative method of describing the same structure is presented with reference to Fig. 11. In such alternative method, masses 12, 14 and 16 together comprise a substrate 200. Substrate 200 has an upper surface 17 coincident with a surface of silicon nitride layer 16.

Yet another alternative method of describing the embodiment of Figs. 11-17 is as follows, and is described with reference to Fig. 11. First, it is recognized that openings 22, 24, 26, 28 and 30 have a periphery bounded by bottom surfaces 220. Steps 222 are then defined between bottom surfaces 220 and upper surface 17 of silicon nitride layer 16. Steps 222 can be referred to as elevational steps formed relative to a substrate, and comprising uppermost surfaces corresponding

to surface 17. In the shown embodiment, steps 222 comprise substantially vertical sidewalls. Material 100 is formed proximate steps 222 and extends to above the elevational step uppermost surfaces 17. Interface 106 extends to at or below an elevational level of the elevational step uppermost surfaces 17.

In this alternative method of description, the processing of Fig. 12 can be referred to as polishing material 100 down to about the elevational level of the elevational step uppermost surface 17, or, in alternative embodiments, as polishing the material down to about the elevational level of interface 106.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.